Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.034”**

**ANODE**

**.023 x .023”**

**.034”**

**Top Material: Ti/Ag**

**Backside Material: Cr/Ni/Ag**

**Bond Pad Size: .028” X .028”**

**Backside Potential: CATHODE**

**Mask Ref: CPZ25**

**APPROVED BY: DK DIE SIZE .034” X .034” DATE: 6/28/23**

**MFG: CENTRAL SEMI THICKNESS .008” P/N: 1N5918**

**DG 10.1.2**

#### Rev B, 7/1